New AXIe-based Protocol Test Modules for MIPI D-PHY Test

AXIe test solutions expand from computing busses towards mobile computing interfaces

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In the last three decades, the PC industry has been fueling an ecosystem of standardized high speed interconnects - PCI Express, DDR, USB, Sata ,and more - between the various building blocks of typical computer architectures. Standardized busses help reduce design costs, build flexible and scalable configurations to meet various cost and performance needs, and accelerate system integration.

The fast growing mobile computer industry is facing the same technology forces with the emergence of standard interfaces defined by industry alliances such as MIPI (Mobile Industry Processor Interface).

As within the PC industry, the chip to chip connections have undergone an architectural shift from proprietary parallel buses to serializer/deserializer (SERDES) links for several reasons. Serial links eliminate parallel-bus clock skew, reduce the number of pins and traces, and enable power savings with bus sleep modes.

Gigabit serial and packet based interfaces such as MIPI D_PHY CSI (Camera Serial Interface) and DSI (Display Serial Interface) are rapidly emerging as the next generation serial interface between chipsets and LCD display and Cameras within next generation Mobile Handsets. The ongoing evolution of these serial standards introduces multiple levels of complexity in test due to a more complex protocol stack and faster and wider multilane serial links.

The specific nature of the signaling level is such that most general-purpose measurement tools cannot understand specific signals and information encoding so can therefore provide only raw information about the digital data, preventing the designer from getting full insight on his application.

From turn-on through integration, the ability to gain greater confidence in these new designs depends on obtaining deeper insights that span the digital, protocol and bitmap domains. Within each mobile device, new insight begins in the digital domain at the physical and protocol layers, followed by the video application layer.

Mobile designers are adding multiple high-definition cameras and displays, and are beginning to integrate 3-D technology. This increasing demand for bandwidth has driven the expansion of the D-PHY interface specification to include multiple lanes, each one working at 1.5 Gbs. Since 2010, test and measurement equipment manufacturers have leveraged the AXIe architecture to build logic and protocol test solutions for high speed computer interfaces such as DDR and PCI Express. The AXIe module space and power budget fits well with the analysis and emulation requirements for these high speed busses.

The introduction of the Agilent U4421A MIPI D-PHY analyzer and exerciser for mobile applications demonstrates that the AXIe form factor can successfully be used to build test

solutions for a wide range of industry segments, including computing, aerospace defense and now mobile computing applications.

The modular AXIe form factor allows multiple busses to be exercised or analyzed simultaneously. Multiple CSI or DSI busses can be time-correlated with PCIe, DDR, HDMI or a generic high-speed logic analyzer module. Modularity extends to the instrument configuration, and helps build the right solution for every test need.